REMARKS/ARGUMENTS

No new matter has been added. The Office Action mailed July 22, 2004, has been received and reviewed. Claims 1 through 9 and 12 through 19 are currently pending in the application. Claims 1 through 9 and 12 through 19 stand rejected. Applicant has amended claims 1 and 13, and respectfully requests reconsideration of the application as amended herein.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 6,427,194 B1 to Owen et al., in View of U.S. Patent No. 5,469,208 to Dea, and Further in View of U.S. Patent No. 6,040,845 to Melo et al.

Claims 1 through 3, 5 through 9, and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Owen et al. (U.S. Patent No. 6,427,194 B1) in view of Dea (U.S. Patent No. 5,469,208) and further in view of Melo et al. (U.S. Patent No. 6,040,845). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 1 through 3, 5 through 9, and 12 are improper because the elements for a *prima facie* case of obviousness are not met to establish a *prima facie* case of obviousness regarding the presently claimed invention. Specifically, the rejection of the presently claimed invention fails to meet the criterion that the prior art references must teach or suggest all the claim limitations and the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure, to establish a *prima facie* case of obviousness.

Specifically, Applicants' amended independent claim 1 recites:

> 1. A method for compressing video data in a computer system comprising:
>
> receiving a current video frame at a dedicated video input of a core logic chip in the computer system directly from a video source originating the video frame, the computer system including the core logic chip for directly coupling a processor to a system memory and for coupling the processor and the system memory to a system bus;
>
> ***computing at the core logic chip a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input of the core logic chip, the previous video frame being received at the core logic chip as a previous current video frame and retained therein,*** the difference frame including computing the difference frame in the core logic chip within the computer system, wherein the core logic chip is a north bridge chip;
>
> storing the difference frame directly from the core logic chip to the system memory in the computer system via a dedicated memory interface therebetween; and
>
> the processor retrieving the difference frame directly from the system memory via the core logic chip using a dedicated processor interface therebetween to complete compression of the video data. (Emphasis added.)

The Office Action concedes:

> ..., Owen et al explicitly do not disclose: 1) the claimed computing at the core logic chip a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input of the core logic chip the difference frame including computing the difference frame in the core logic chip within the computer system, and . . .. (Office Action, p. 3).

The Office Action continues by alleging:

> 1) Dea teaches that a frame subtraction is perform[ed] in difference block 220 when compression/decompression accelerator 120 performs motion estimation encoding, in the subtraction of frame difference block 220, the information of reference frame line 209 is subtracted from the current frame information on current frame line 205, the difference between the reference frame data of line 209 and the current frame data of line 205 is then provided for encoding at the output of frame difference block 220 (Fig. 2, col. 5, line 24 to col. 10, line 21). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the compression/decompression accelerator which has frame difference block 220 as taught by Dea into Owen et al's system in order to provide the hardware circuitry for performing video encoding and decoding operation." (Office Action, pp. 3-4).

Applicants respectfully disagree with the Office Action's characterization of the teachings of Dea. Specifically, Dea teaches or suggests a compression/decompression accelerator 120 which includes a frame difference block 220 for calculating a difference frame from current frame memory 204 and previous frame memory 206 wherein "[a]ll RAM within accelerator 120 must read and write by way of accelerator bus interface 200."(Col. 5, lines 40-42). Such an architecture is clearly visible with reference to FIGS. 1 and 2 where the frame difference block 220 is only accessible by way of bus interface 200 which retrieves the values from the current frame memory 204 and the previous frame memory 206 which where previously stored there. Therefore, the frame difference block 220 of Dea can only be fed frame data for calculating a difference frame from data that has been stored in memory 114 and not, as claimed by Applicants, by "receiving a current video frame at a dedicated video input of a core logic chip . . . directly from a video source originating the video frame . . .;" and "***computing at the core logic chip a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input of the core logic chip, the previous video frame being received at the core logic chip as a previous current video frame and retained therein,*** . . .." (Emphasis added.)

The Office Action cites Melo et al for "teach[ing] that using conventional master/slave nomenclature, the graphics accelerator can be considered an AGP compliant master, the north bridge, and specifically, the memory controller or core logic within the north bridge can be partially considered as an AGP compliant target . . ." (Office Action, p. 4.), which does not provide any further teaching or suggestion for the claim limitations as previously stated.

Applicants submit that since none of the references teach, suggest or motivate Applicants' invention as claimed in amended independent claim 1, the rejection should be withdrawn and claims 1 through 3, 5 through 9, and 12 passed to allowance.

Obviousness Rejection Based on U.S. Patent No. 6,427,194 B1 to Owen et al., in View of U.S. Patent No. 5,469,208 to Dea, U.S. Patent No. 6,040,845 to Melo et al., and Further in View of U.S. Patent No. 4,546,383 to Abramatic et al.

Claims 4 and 13 through 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Owen et al. (U.S. Patent No. 6,427,194 B1) in view of Dea (U.S. Patent No. 5,469,208), Melo et al. (U.S. Patent No. 6,040,845), and further in view of Abramatic et al. (U.S. Patent No. 4,546,383). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 4 and 13 through 19 are improper because the elements for a *prima facie* case of obviousness are not met to establish a *prima facie* case of obviousness regarding the presently claimed invention. Specifically, the rejection of the presently claimed invention fails to meet the criterion that the prior art references must teach or suggest all the claim limitations and the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure, to establish a *prima facie* case of obviousness.

Regarding claim, Applicants respectfully assert that claim 4 depends from amended independent claim 1 and reassert the above proffered arguments in support of the allowability of amended independent claim 1. Applicants request the rejection of claim 4 be withdrawn based at least on its dependency on amended independent claim 1.

Regarding amended independent claim 13, from which dependent claims 14 through 19 depend, Applicants assert that amended independent claim 13 recites:

13. A method for compressing video data in a computer system, comprising:
receiving a current video frame at a dedicated video input of a core logic chip in the computer system directly from a video source originating the video frame, the computer system including the core logic chip for directly coupling a processor to a system memory and for coupling the processor and the system memory to a system bus;
computing at the core logic chip a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input of the core logic chip, the previous video frame being received at the core logic chip as a previous current video frame and retained therein, the difference frame including computing an exclusive-OR between the current video frame and the previous video frame, and wherein computing the difference frame includes computing the difference frame in the core logic chip within the computer system, wherein the core logic chip is a north bridge chip;
storing the difference frame directly from the core logic chip into the system memory in the computer system via a dedicated memory interface therebetween;
storing the current video frame directly from the core logic chip into the system memory in the computer system using a dedicated processor interface therebetween;
the processor retrieving the difference frame directly from the system memory via the core logic chip; and
compressing the video data using the difference frame to produce compressed video data. (Emphasis added.)

The Office Action concedes:

> ..., Owen et al explicitly do not disclose: 1) the claimed computing at the core logic chip a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input of the core logic chip the difference frame including computing the difference frame in the core logic chip, 2) the claimed wherein the core logic chip is a north bridge chip, and 3) the claimed the difference frame including computing an exclusive-OR between the current video frame and the previous video frame, the wherein computing the difference frame includes computing the difference frame in the core logic chip within the computer system. (Office Action, p. 8).

The Office Action continues by alleging:

> 1) Dea teaches that a frame subtraction is perform[ed] in difference block 220 when compression/decompression accelerator 120 performs motion estimation encoding, in the subtraction of frame difference block 220, the

> information of reference frame line 209 is subtracted from the current frame information on current frame line 205, the difference between the reference frame data of line 209 and the current frame data of line 205 is then provided for encoding at the output of frame difference block 220 (Fig. 2, col. 5, line 24 to col. 10, line 21). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the compression/decompression accelerator which has frame difference block 220 as taught by Dea into Owen et al's system in order to provide the hardware circuitry for performing video encoding and decoding operation." (Office Action, pp. 8-9).

As stated above and reiterated herein, Applicants respectfully disagree with the Office Action's characterization of the teachings of Dea. Specifically, Dea teaches or suggests a compression/decompression accelerator 120 which includes a frame difference block 220 for calculating a difference frame from current frame memory 204 and previous frame memory 206 wherein "[a]ll RAM within accelerator 120 must read and write by way of accelerator bus interface 200."(Col. 5, lines 40-42). Such an architecture is clearly visible with reference to FIGS. 1 and 2 where the frame difference block 220 is only accessible by way of bus interface 200 which retrieves the values from the current frame memory 204 and the previous frame memory 206 which where previously stored there. Therefore, the frame difference block 220 of Dea can only be fed frame data for calculating a difference frame from data that has been stored in memory 114 and not, as claimed by Applicants, by "receiving a current video frame at a dedicated video input of a core logic chip . . . directly from a video source originating the video frame . . .;" and "***computing at the core logic chip a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input of the core logic chip, the previous video frame being received at the core logic chip as a previous current video frame and retained therein,*** . . .." (Emphasis added.)

The Office Action cites Melo et al for "teach[ing] that using conventional master/slave nomenclature, the graphics accelerator can be considered an AGP compliant master, the north bridge, and specifically, the memory controller or core logic within the north bridge can be partially considered as an AGP compliant target . . ." (Office Action, p. 9.), which does not provide any further teaching or suggestion for the claim limitations as previously stated.

Applicants submit that since none of the references teach, suggest or motivate Applicants' invention as claimed in amended independent claim 13, the rejection should be withdrawn and claims 13 through 19 passed to allowance.

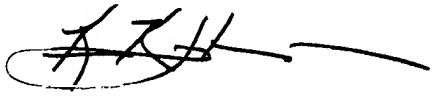
ENTRY OF AMENDMENTS

The amendments to claims 1 and 13 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 1 through 9 and 12 through 19 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,



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Date: October 12, 2004
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